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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,626	01/24/2002	Andrew Moroney	13453-002001	2191

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EXAMINER	
SERRAO, RANODHI N	

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,626	MORONEY ET AL.	
	Examiner	Art Unit	
	Ranodhi Serrao	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/16/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6, 7, 8, 9, and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "said instruction-memory pointer" and "said selected instruction word" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "said selected instruction word" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 8 recites the limitation "said selected instruction word" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 9 recites the limitation "said instruction-memory pointer" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "said instruction-memory pointer" in line 5 of the claim and recites the limitation "said instruction-memory pointer" in line 8 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Gallup et al. (5,572,689).

As per claim 1, Gallup et al. teaches a system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, at least one of said first and second networks being a storage area network (column 119, lines 15-26: wherein the neural network serves the function of a storage area network), said system comprising: a first data port for receiving input data from said first network said input data being expressed in said first network protocol; a second data port for receiving state information indicative of a state of a first storage area network selected from said first and second networks (column 24, lines 55-62 and column 29, lines 53-63): wherein it is obvious to one of ordinary skill in the art to add a second network reading from the above reference); and a microsequencer system configured to translate said input data on the basis of said state information, said microsequencer system translating said input data into corresponding data expressed in said second network protocol (column 43, lines 42-49).

As per claim 2, Gallup et al. teaches at least one programmable microsequencer (column 82, lines 25-44).

As per claim 3, Gallup et al. teaches a microsequencer (column 82, lines 25-44).

As per claim 4, Gallup et al. teaches a plurality of microsequencers configured to cooperate in translating said input data into corresponding data expressed in said

second network protocol (column 124, lines 48-64: wherein decoding serves the function of translating).

As per claim 5, Gallup et al. teaches an instruction memory accessible to a constituent microsequencer of said microsequencer system, said instruction memory having a plurality of instruction words, each of said instruction words having sufficient length to hold at least two instructions (column 119, lines 4-13); and an instruction-memory pointer for identifying a selected instruction word in said instruction memory (column 48, lines 10-14).

As per claim 6, Gallup et al. teaches a translation-memory accessible to a constituent microsequencer of said microsequencer system, said translation-memory having a translation-memory address (column 46, line 66-column 47, line 3), and a translation-memory element corresponding to said translation-memory address, said translation-memory element including data for causing said instruction-memory pointer to jump to said selected instruction word (column 72, lines 34-46).

As per claim 7, Gallup et al. teaches an absolute address of said selected instruction word (column 39, lines 39-45).

As per claim 8, Gallup et al. teaches an offset from a current instruction word to said selected instruction word (column 39, lines 39-45).

As per claim 9, Gallup et al. teaches a translation-memory pointer for indirectly causing said instruction-memory pointer to jump to a selected instruction-memory address (column 47, lines 10-17).

As per claim 10, Gallup et al. teaches said translation-memory pointer is configured to identify a selected translation-memory address corresponding to a translation-memory element that contains data indicative of said selected instruction-memory address (column 75, lines 42-54: wherein decoding serves the function of translating).

As per claim 11, Gallup et al. teaches a translation-memory having: a translation-memory address (column 46, line 66-column 47, line 3); a first translation-memory element corresponding to said translation-memory address, said first translation-memory element including data for causing said instruction-memory pointer to jump to a first instruction word (column 72, lines 34-46); a second translation-memory element corresponding to said translation-memory address, said second translation-memory element including data for causing said instruction-memory pointer to jump to a second instruction word (column 72, lines 34-46: wherein it is obvious to one of ordinary skill in the art to add a second translation-memory element reading from the above reference); and a selector for selecting said first translation-memory element (column 124, lines 48-64: wherein decoding serves the function of translating).

As per claim 12, Gallup et al. teaches a multiplexer having a first multiplexer input for receiving data indicative of content of said first translation-memory element (column 111, lines 23-42); a second multiplexer input for receiving data indicative of content of said second translation-memory element (column 111, lines 23-42: wherein it is obvious to one of ordinary skill in the art to add a second multiplexer input from reading the above reference); an output providing data selected from at least said first

multiplexer input and said second multiplexer input (column 129, lines 20-31); and a control input for controlling data provided at said output (column 129, lines 20-31).

As per claim 13, Gallup et al. teaches an output port in communication with said microsequencer system for providing said corresponding data to said second network (column 126, line 63-column 127, line 5).

As per claim 14, Gallup et al. teaches said first and second data ports and said microsequencer system are integrated into one integrated circuit (column 104, line 6-column 105, line 10).

As per claim 15, Gallup et al. teaches a system for enabling communication between a first network having a first network protocol and a second network having a second network protocol (column 24, lines 17-34 and column 24, lines 52-62), said system comprising: a first input port for receiving input data from said first network (column 78, lines 1-8); a second input port for receiving state information associated with said first network (column 79, lines 13-20); a processing element in communication with said first and second input ports (column 82, lines 25-44: wherein the microsequencer serves the function of a processing element); an instruction memory accessible to said processing element, said instruction memory having a plurality of instruction words, each of said instruction words having sufficient length to hold at least two instructions, said plurality of instruction words being selected to translate input data from said first protocol to said second protocol (column 119, lines 4-13); and an instruction-memory pointer for identifying a selected instruction word in said instruction memory (column 48, lines 10-14).

As per claim 16, Gallup et al. teaches said processing element is selected from the group consisting of: a microsequencer system having at least one microsequencer; a micro-processor; and an application-specific integrated circuit (column 42, lines 16-20 and column 104, line 60-column 105, line 10).

As per claim 17, Gallup et al. teaches a processing system comprising: a processing element (column 82, lines 25-44: wherein the microsequencer serves the function of a processing element); an instruction memory accessible to said processing element, said instruction memory having an associated instruction-memory pointer for identifying a selected instruction word in said instruction memory (column 119, lines 4-13); and a translation-memory accessible to said processing element, said translation-memory having a translation-memory element identified by a translation-memory address, said translation-memory element including data for causing said instruction-memory pointer to jump to said selected instruction word (column 72, lines 34-46).

As per claim 18, Gallup et al. teaches a translation-memory pointer for indirectly causing said instruction-memory pointer to jump to a selected instruction-memory address (column 72, lines 34-46).

As per claim 19, Gallup et al. teaches said translation-memory pointer is configured to identify a selected translation-memory address that corresponds to a translation-memory element containing data indicative of said selected instruction-memory address (column 75, lines 42-54: wherein decoding serves the function of translating).

As per claim 20, Gallup et al. teaches said translation-memory element is configured to include an absolute address of said selected instruction word (column 39, lines 39-45).

As per claim 21, Gallup et al. teaches said translation-memory element is configured to include an offset from a current instruction word to said selected instruction word (column 39, lines 39-45).

As per claim 22, Gallup et al. teaches said instruction memory includes a plurality of instruction words, each of said instruction words having sufficient length to hold at least two instructions (column 119, lines 4-13).

As per claim 23, Gallup et al. teaches said processing element is selected from the group consisting of a microsequencer system having at least one microsequencer, a microprocessor, a microcontroller, and an application-specific integrated circuit (column 42, lines 16-20 and column 104, line 6-column 105, line 10).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Padovano (6,606,690) teaches a system and method for accessing a storage area network as network attached storage. Cooper et al. (5,809,527) teaches an outboard file cache system. Byers et al. (5,535,405) teaches a microsequencer bus controller system. Starr et al. (6,807,581) teaches an intelligent network storage interface system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ranodhi Serrao whose telephone number is (571)272-7967. The examiner can normally be reached on 8:00-5:30pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on (571)272-3880. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER